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LOW POWER, RADIATION HARD GaAs RAM

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The scope of this program is to demonstrate a 1K GaAs static RAM having very low power dissipation and short access time to meet the requirements of the DARPA Advanced On-Board Signal Processer (AOSP). In the six months covered by this report device isolation and backgating studies were performed, subthreshold uniformity measurements made, and a new RAM design using transmission gates finalized.

Proton damage has proven to be an effective technique for maximizing device isolation for ultra-low power RAM circuits. However, backgating still remains as a possible yield limiting factor. Backgating measurements have been performed on test structures to determine the influence of backgating in proton isolated material with differing acceptor content. The results have been used to refine models for backgating and to identify properties of the starting GaAs material which affect backgating and isolation.

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A technique to characterize FET devices within a RAM has been successfully developed. It applies to test arrays of 224 (16 x 14) RAM cells extracted from the 1K RAM, and which have each row word-line, and each column bit-sense line connected to a contact pad. With a proper biasing scheme, and using our parametric test system, the subthreshold characteristic of the output FET in each of the 72 cells forming the central core of the array can be measured individually. The device characteristics appear uniform and well behaved, as expected from measurements on single devices.

The design of a transmission gate RAM has been completed and will be implemented on the RM5 mask set. The overall dimensions of this circuit are 1600 x 1600 μm with a cell size of 43 x 63 μm. The RAM is 256 bits, configured as 256 x 1, in 16 rows and 16 columns. Estimated cell power is 3.5 μW/bit.

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1.0 INTRODUCTION

The development of a low power, radiation hard memory chip is motivated by the DARPA Advanced On-Board Signal processor (ASOP) program. The goal of this program is to develop a flexible, multimission signal processor to fulfill the processing requirements of space-based missions through the 1990's. The ASOP system specification translates into memory device specifications in the following manner. Long mission lifetimes (> 5 years) and space-based environmental conditions require a radiation hardened device technology capable of surviving total doses in excess of 10^6 rads. Power dissipations of 0.5-1 μW/bit are required due to the large memory sizes and limited power budget. The 4K memory design goals are summarized in Table 1.1.

Table 1.1
AOSP GaAs Memory Design Goals

Memory Type	Static Random Access
Power Dissipation	1 μW/bit
Speed	τ_{access} < 10 ns
Radiation Hardness	> 10^6 rad total dose
Storage Capacity	4096 bits/chip

The above requirements are very demanding. They represent a "speed power" product of < 10 fJ/bit.

In the previous GaAs static RAM development program, a low power RAM cell was designed and a 256 bit RAM was demonstrated. The final phase of the previous program provided an opportunity to begin processing 3 in. GaAs wafers. The implementation of the 3 in. wafer process was very successful.

In this report, the results from the third semester of a 21-month program designed to raise the complexity of the GaAs static RAM from 256 to 1K bits with the operating characteristics listed in Table 1.1 are discussed. In particular, isolation and backgating will be discussed since these factors are major yield limiting parameters. Also, subthreshold uniformity will be discussed and correlation will be attempted between cell failure and transistor characteristics. Finally, new RAM devices incorporated on the RM5 mask set will be described in detail.

2.0 ISOLATION AND BACKGATING STUDIES IN GaAs

In as-grown undoped LEC GaAs substrate material, typical resistivities in the range 10^7-10^8 Ω-cm are observed. However, following ion implantation and annealing procedures used to fabricate GaAs MESFET devices, carrier conduction processes become dominated at relatively low voltages by space-charge injection for contact spacings less than 20 μm. The space-charge injection can lead to loss of isolation and backgating effects which significantly effect device performance and yield in GaAs IC's.

To eliminate these space-charge injection effects, devices are isolated using a proton bombardment step in the IC fabrication process. The proton bombardment effectively eliminates space-charge injection in a surface damage region roughly 1 μm deep. The proton isolation step is a high yield step since many devices will still function even if particulates or lithography errors have prevented proton penetration into the GaAs surface regions.

For low power devices, such as GaAs static RAMs using depletion mode devices, the isolation is critical to yield since leakage currents on the order of 100 nA can prevent memory cells from holding data. For design purposes, the temperature range over which this isolation is effective must be established. In addition, the degree of backgating (or sidegating) in material which has been proton isolated needs to be determined. Previous studies have indicated that leakage currents and backgating thresholds could be correlated with each other. In this report both issues have been addressed. The I-V characteristics of proton isolated layers have been studied between 25°C and 115°C. Backgating measurements have been performed on test structures to determine the influence of backgating in proton isolated material with differing acceptor content. These results have been used to refine models for backgating and to identify properties of the starting GaAs substrate material which affect backgating and isolation.

2.1 Temperature Dependence of Isolation

Proton irradiation of GaAs produces both deep donor levels and deep acceptor levels which compensate shallower levels and pin the Fermi level near midgap. For high dose proton implants (> 10^{14} cm^{-2}), the reduced mobility produces a high resistivity region. Since the ionization of deep donor levels typically determines the carrier concentration in proton isolated layers, and since these levels are relatively deep (0.6-0.8 eV) with respect to the conduction band, a large temperature dependence of the resistivity is expected. To lowest order the conductivity can be approximated as

$$\sigma = ne\mu = e\mu\gamma \frac{N_{DD} N_C(T)}{N_{DA}} e^{-E_{DD}/kT} \qquad (1)$$

where e is the electronic charge, μ is the mobility, N_{DD},N_{DA} are the densities of deep donors and deep acceptors, $N_C(T)$ is the effective density of states in the conduction band, E_{DD} is the energy of the defect at which the Fermi level is pinned and ξ is the ratio of degeneracy factors for the donors and acceptors. At room temperature the sheet resistance for a typical structure exceeds 10^{10} Ω/sq. However, at elevated temperatures the sheet resistance becomes much less due to the exponential factor in Eq. (1).

To determine the temperature dependence, I-V measurements were performed at different temperatures in the range 25°C to 115°C. The structure used was a 3 μm isolation gap placed between two 50 μm × 50 μm pads of ohmic metal alloyed on the wafer. These structures were test patterns on a normal GaAs IC wafer lot. The results of these measurements are shown in Fig. 1. An exponential dependence is observed with a thermal activation energy of E_{DD} ≈ 0.70 eV. This energy is close to the energy associated with anion antisite As_{Ga} defects and suggests that antisite defects and/or antisite-other defect complexes may play a major role in determining the conductivity in the proton damaged regions. Such defects are commonly observed in GaAs which has been ion-damaged.

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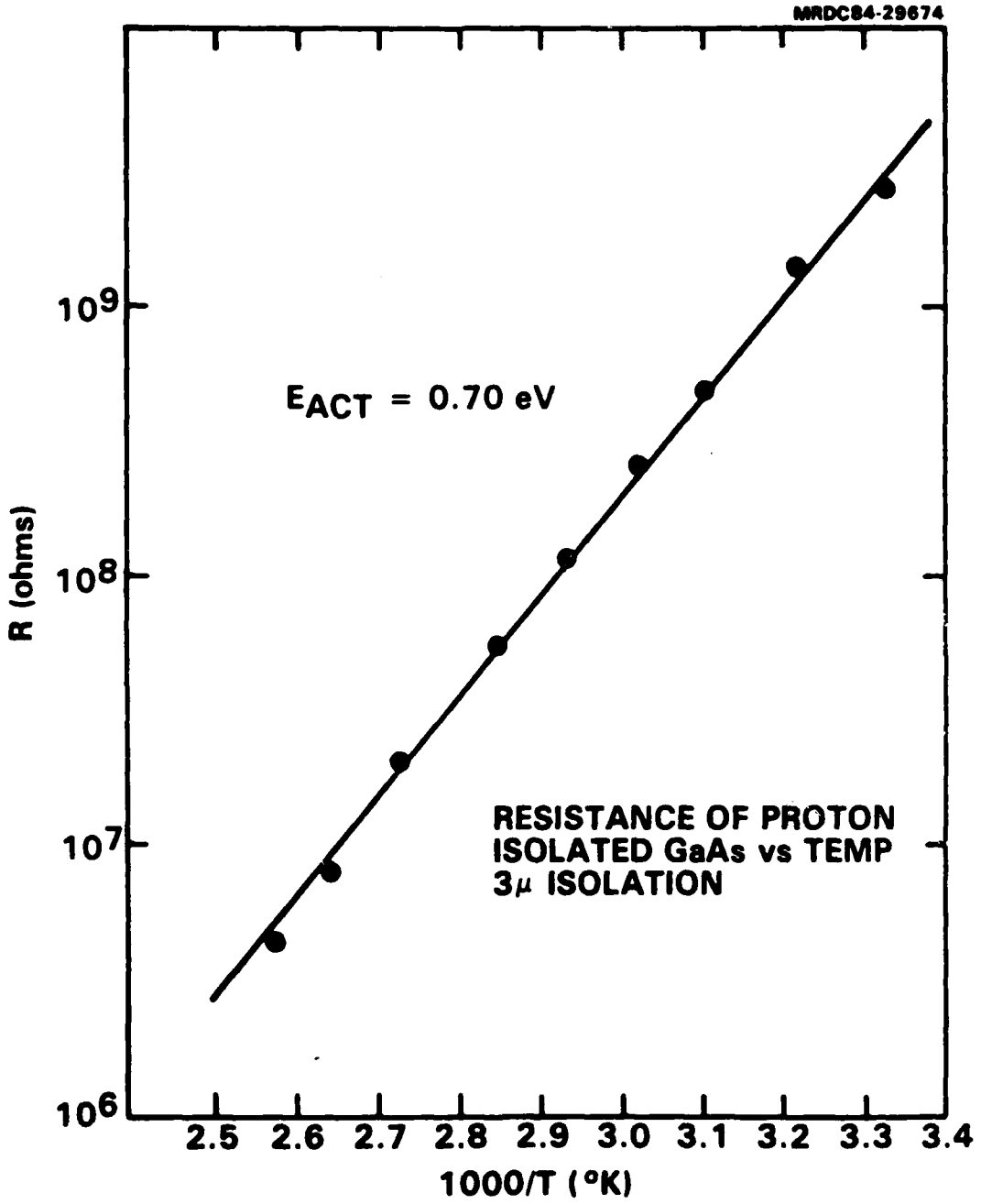

Fig. 1 Resistance of proton-isolated GaAs 3 μm gap between 50 μm long ohmic.

At 112°C the resistivity has decreased by roughly three orders of magnitude from room temperature to approximately 7×10^7 Ω/sq. Although the resistivity has dropped, it is still sufficiently large to provide adequate isolation for most purposes. The exception is for circuits with extremely large load resistances. To operate with adequate voltage swing, such a circuit must have a load resistance substantially less than the effective resistance of the substrate. Assuming 0.1 sq. in a typical case and a safety margin of a factor of five, this places an upper limit of 1 MΩ for load resistances in standard gate configurations for operation up to 125°C.

The effective sheet resistivity of the substrate typically varies by only a factor of two before and after protons. Hence, the contribution of the undamaged GaAs regions will affect the conductivity substantially. This component has a similar exponential dependence on temperature and cannot be separated from conduction in the proton damaged region. Since conduction in the damaged region is inherently three-dimensional, care must be used when estimating the amount of conduction between contacts since conduction is not confined only to a thin sheet near the surface, and sheet scaling rules may not apply.

2.2 Backgating and Sidegating in Proton Damaged Material

In the proton damaged material, space-charge injection is occasionally observed but only at relatively high electric fields (10^4-10^5 V/cm). For normal BFL and SDFL supply voltages and for standard circuit layout and design, such large fields are never obtained. Therefore, substrate conduction can be treated as ohmic in most practical cases. Even though the isolation has been improved, the degree of backgating obtained still varies a great deal from wafer to wafer.

To verify a mechanism for backgating, several studies were performed. A literature search shows that the residual acceptor content of the substrate may affect the degree of backgating. In addition, the outdiffusion of EL2 deep donors almost certainly plays a role in the degree of backgating observed.

To test the role of residual acceptor content on backgating, leakage studies were performed on a structure consisting of a standard 10 μm MESFET with an ohmic contact 20 μm in length perpendicular to the gate of the MESFET at a distance of 7 μm. All nonactive regions in the structure were proton isolated with a 1.5E14 cm^{-2} 100 KeV proton isolation step. These structures were measured on nine different wafers with known carbon content. Also on these wafers were Schottky diode test structures for C-V measurements. To represent a worst-case scenario for high density circuits, the distance from the backgate electrode to the FET (7 μm) was less than used in previous measurements (26 μm).

To measure backgating, the drain current at fixed drain-source voltage (2.0 V) was monitored as a function of the backgating electrode voltage. The current through the backgating electrode was also monitored. The gate of the FET was grounded to the source.

Typical results of these measurements are shown in Figs. 2 and 3. The leakage current in all cases is comparatively small compared to prior proton isolation being less than 6 nA at 5 V bias. In all cases the leakage is dominated by ohmic conduction and is similar to the curves shown in Figs. 2 and 3. Zero net current flow is obtained at 1 V forward bias, roughly half the drain-source bias, indicating symmetric current flow to the drain and source regions.

Although the leakage current in these structures is fairly reproducible and well behaved, the backgating properties are highly irregular between different wafers. No clear association with the material properties could be made, although material with lower carbon content generally showed higher backgating thresholds than material with low carbon content. For instance, the material used for measurements shown in Fig. 2 had undetectable carbon levels and showed very little backgating. The material used for the measurements shown in Fig. 3 had 1.1×10^{16} cm^{-3} and showed moderately strong backgating. Material with carbon content $> 3 \times 10^{16}$ showed severe backgating. However, some material with 1×10^{16} cm^{-3} carbon showed little backgating

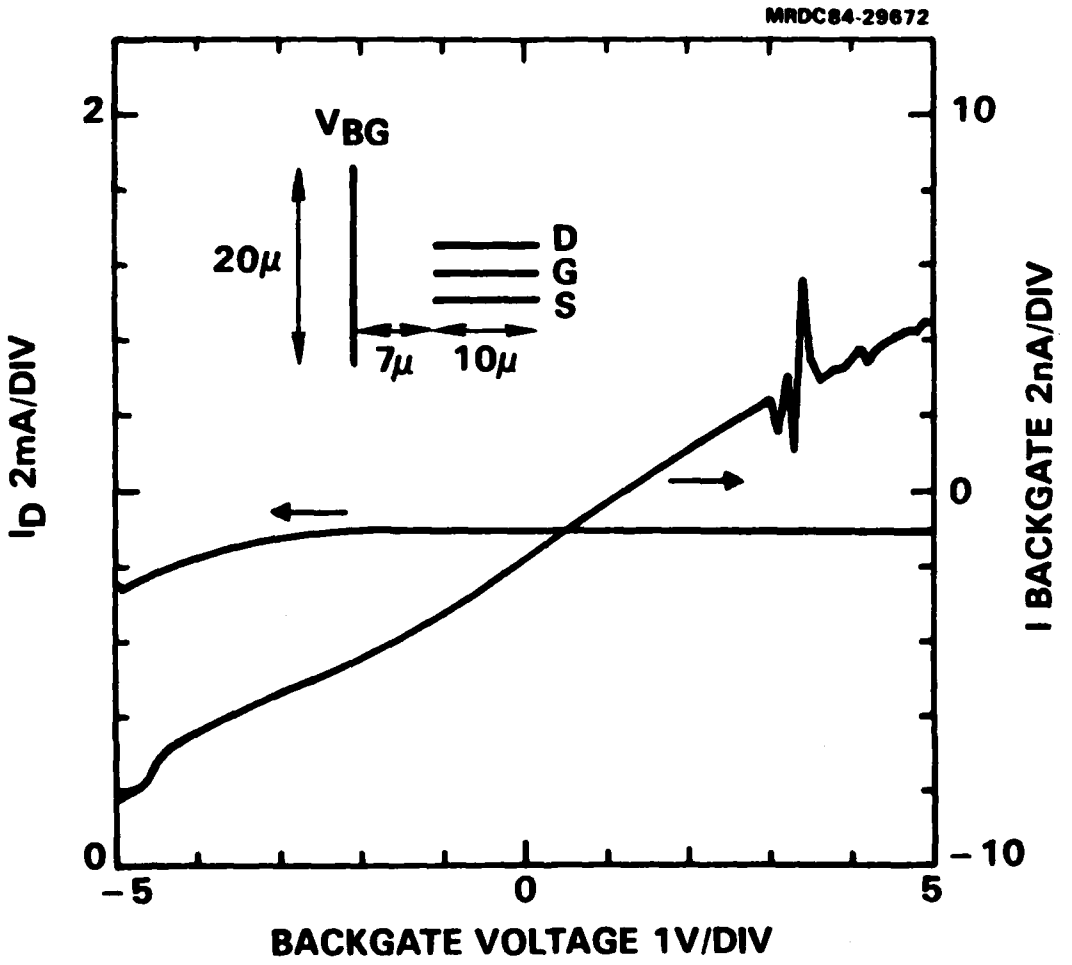

Fig. 2 Backgating in proton-isolated GaAs low carbon ($< 1 \times 10^{15}$ cm^{-3}).

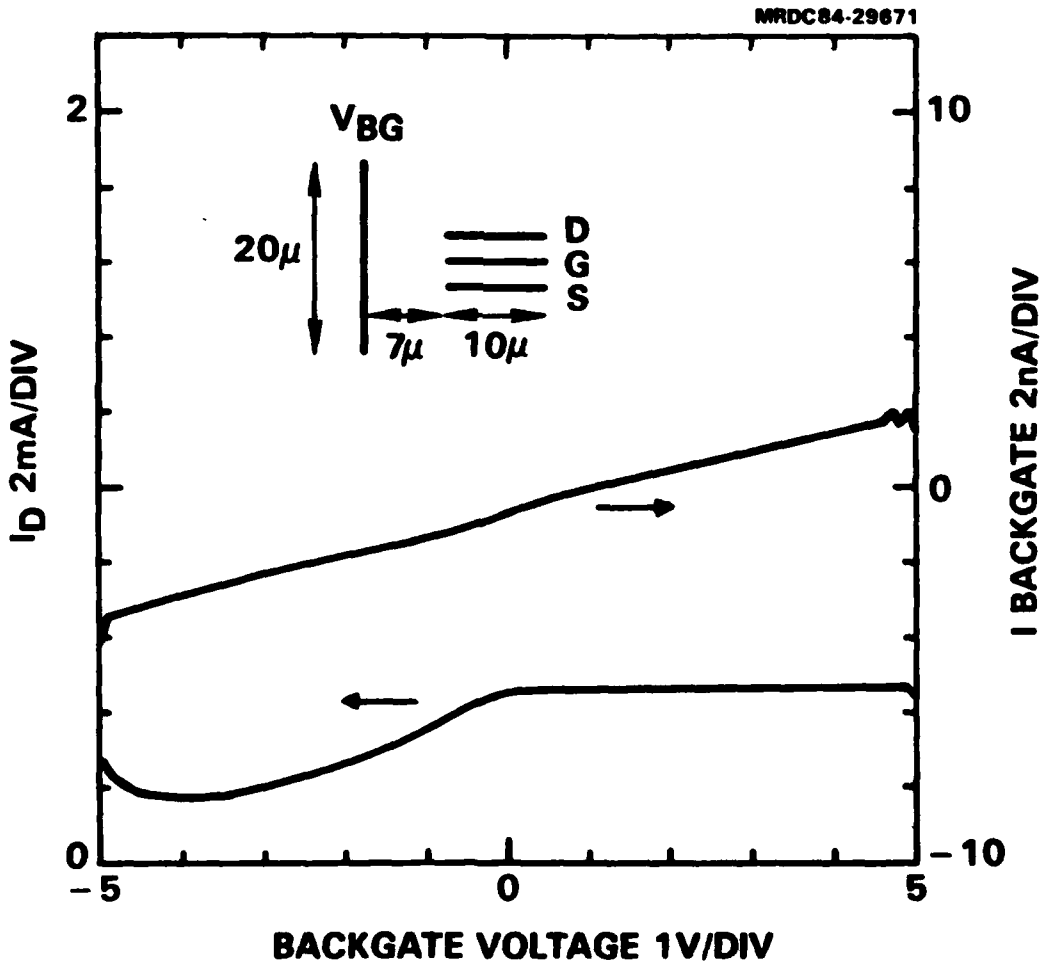

Fig. 3 Backgating in proton-isolated GaAs high carbon (1.25×10^{16} cm^{-3})

indicating that the carbon content alone is not sufficient criteria to establish whether or not backgating will be important in finished wafers.

Backgating characteristics shown in Figs. 2 and 3 had a time-dependent hysteresis with a time constant of several seconds. Such an effect is possible only if trapping plays an important role in the backgating process. Since EL2 (presumably an As_{Ga} antisite or As_{Ga} antisite complex) is the only known trap in substantial concentration in the material used here, charge trapping on ionized EL2 defects must be at least partially responsible for the backgating phenomena. EL2 is known to outdiffuse from bulk LEC material when the material is annealed following implantation. To verify that EL2 is actually outdiffusing, DLTS measurements were made on the implanted Schottky diodes present on the same wafers as the backgating test structures. The concentration of EL2 was found to be a factor of 10 or more lower than measured in the starting material. Typical concentrations ranged from less than 10^{14} cm^{-3} to 2×10^{-15} cm^{-3}, whereas the content in the starting material is typically 2×10^{16} cm^{-3}. These results confirm that substantial EL2 outdiffusion occurs.

Typical data also indicate that backgating is observed only for negative backgating potentials. Since the backgating current is symmetrical one might expect the backgating effect to take place at positive potentials also. This asymmetry in the backgating characteristics suggests that rectifying behavior is occurring at the FET-substrate interface.

A refinement of the backgating model incorporates the results of these studies is indicated in Fig. 4. Outdiffusion of EL2 creates a shallow EL2 layer at the GaAs surface. For low carbon material, this layer will be fully depleted; whereas for high carbon material, the layer may actually be p-type with carrier concentration $\sim 10^{16}$ cm^{-3}. Following proton irradiation, this layer is eliminated except in a shallow region behind the FET channel. The presence of the layer produces a potential well which traps charge on residual EL2 centers in the well region. In high carbon material, the well will become sufficiently deep to form a p-n junction. Since the outdiffusion

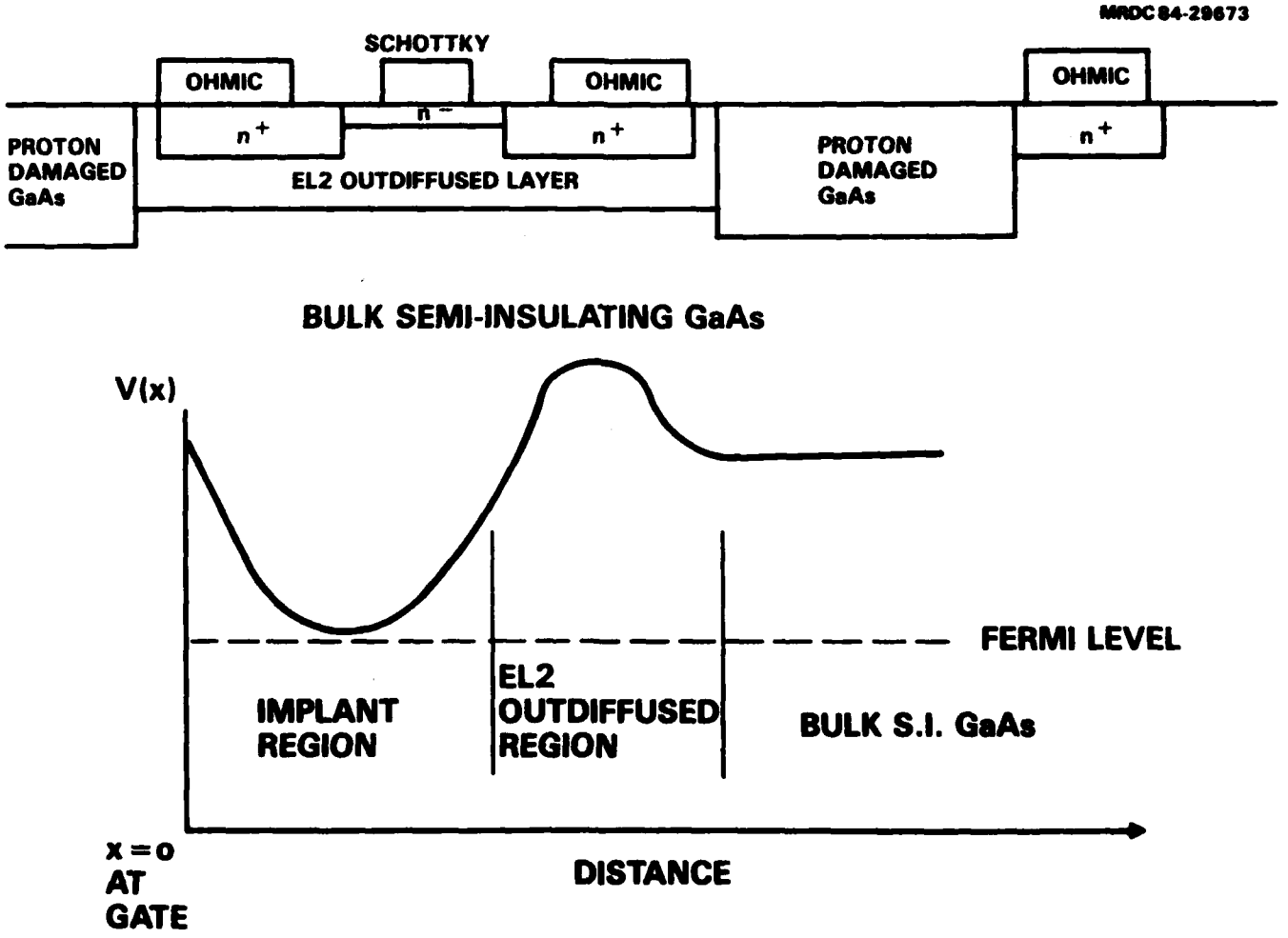

Fig. 4 Backgating in GaAs integrated circuits.

of EL2 can be extremely nonuniform and process dependent, the amount of backgating is highly variable.

To effectively eliminate the presence of the well and hence to minimize backgating, the outdiffusion of EL2 centers and number of residual carbon acceptors should be minimized. Further experiments have been initiated to test this hypothesis.

3.0 MEASUREMENT OF SUBTHRESHOLD CHARACTERISTICS OF MESFETs IN AN UNDECODED RAM CELL ARRAY

Determining the cause for the failure of a cell within a RAM is difficult, unless the failure is due to some lithographic defect which can be detected by microscope observation. Electrical failures are difficult to trace, and very often their cause can only be guessed or inferred. Attempting to address this problem, a technique to probe an individual FET within a RAM array has been successfully developed and applied. The technique has its limitations, it can only reach one of the FETs in the RAM cell, and the cell has to be in an undecoded array. This technique provides a means of observing correlations between cell failures and transistor characteristics.

Figure 5 shows the schematic of the memory cell used in the 1K RAM on mask set RM4 as well as in undecoded arrays of 16 × 14 = 224 cells placed on the same mask set for experimental purpose. The undecoded RAM array is built by stacking cells such as the one shown in Fig. 5. The DATA, $\overline{\text{DATA}}$ and bit sense line connect the cells by columns, and the word line connects the cells by rows. The driver transistor, 10 μm wide, located in the lower right corner of the cell (Fig. 5) has its source connected to the word line; its gate connected to another gate and other internal nodes of the cell; and its drain connected to the bit sense line through a diode. Focusing on these FET drivers and disregarding the rest of the cell, these transistors form a FET array with the sources of the FETs in each row connected to a word line; the drains of the FETs in each column connected to a bit sense line; and the gates of all the FETs tied together through some complex circuitry. If V_{DDA} is left floating, V_{SSA} can be used as the common bias electrode for the gates of the FETs with all the complicated circuitry tied to the gates inactive. V_{SSA} is connected to each FET gate through a 26 MΩ resistor; but this resistance has negligible effect on the measurement of FET characteristics, because it competes with the high gate input impedance of the device. The diodes between the drains of the FETs and the bit sense lines are also negligible because the FET subthreshold characteristics are measured in the saturation region of the characteristics, where a small drain voltage drop has no significant effect.

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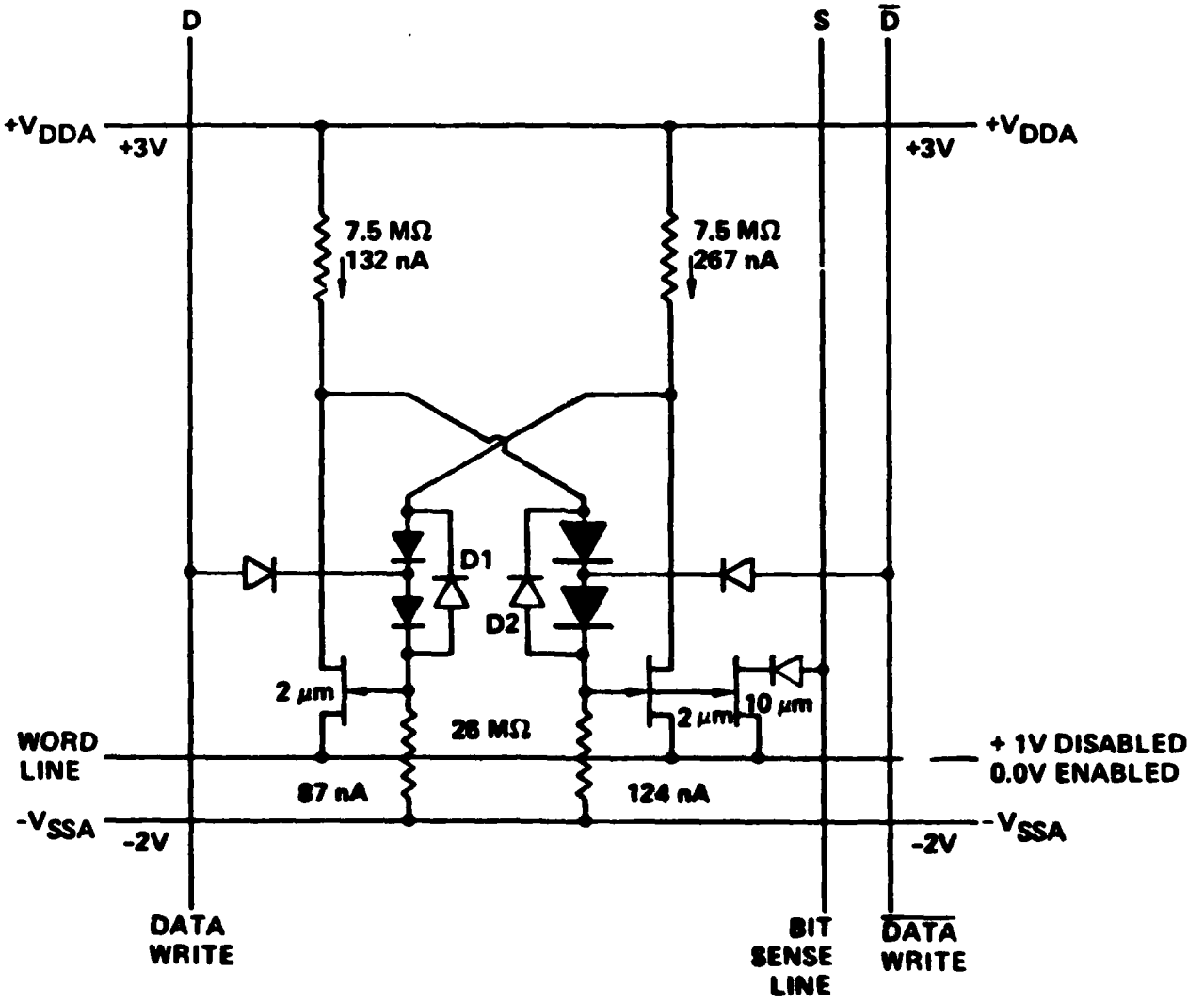

POWER/BIT = (+3) (389) + (2) (211) = 1.6 μw/BIT

Fig. 5 Cell used in 1K GaAs static RAM as well as in subthreshold current measurements.

Once the unused circuitry is conceptually removed, the RAM cell array looks like the FET array shown on Fig. 6. The sources are connected to the horizontal word lines, the drains are connected to the vertical bit sense lines and the gates are all tied together. To address a particular device such as the one circled in Fig. 6, the corresponding column and row are biased at the required V_{ds} and ground, respectively. To turn off the other FET devices in the same row, all the other columns are biased at ground voltage, so that the other FETs have zero bias between drain and source. To turn off the other FETs on the same column, all the other rows are biased at V_{ds}, so that the devices have their drains and sources at the same voltages. Note that a separate power supply V_{ds}^{1} is used to bias the word lines that are turned off, so that any current drawn by this supply does not obscure the measurement of the drain current, I_d, measured at V_{ds}. Equally, the ground connections of the bit sense lines that are not used are also made to a separate ground, so that the ground current of the device under test, I_s, can be measured without ambiguity.

The subthreshold characteristics of the FETs in the arrays were measured using our parametric test system. A computer controlled crosspoint relay matrix takes care of the extensive switching required to address the device one at a time. The bias voltages are applied and the currents are sensed by a Hewlett Packard semiconductor parameter analyzer. All the equipment is controlled by a Data General Lab Microcomputer, and the acquired data are transferred to a Data General MV8000 computer where they are processed. Due to a limitation imposed by the number of relays in our relay matrix, not all the 224 cells in the undecoded RAM array can be addressed. A center core of 9 rows by 8 columns equal to 72 devices was selected. All the other FETs are permanently turned off by nonswitchable connections.

A typical example of the data obtained is shown in Fig. 7. Here drain current is displayed against gate voltage at fixed drain voltages of 2 V. The characteristics of all 72 devices are superimposed. The threshold voltage obtained by standard parametric testing of FETs in test structures on

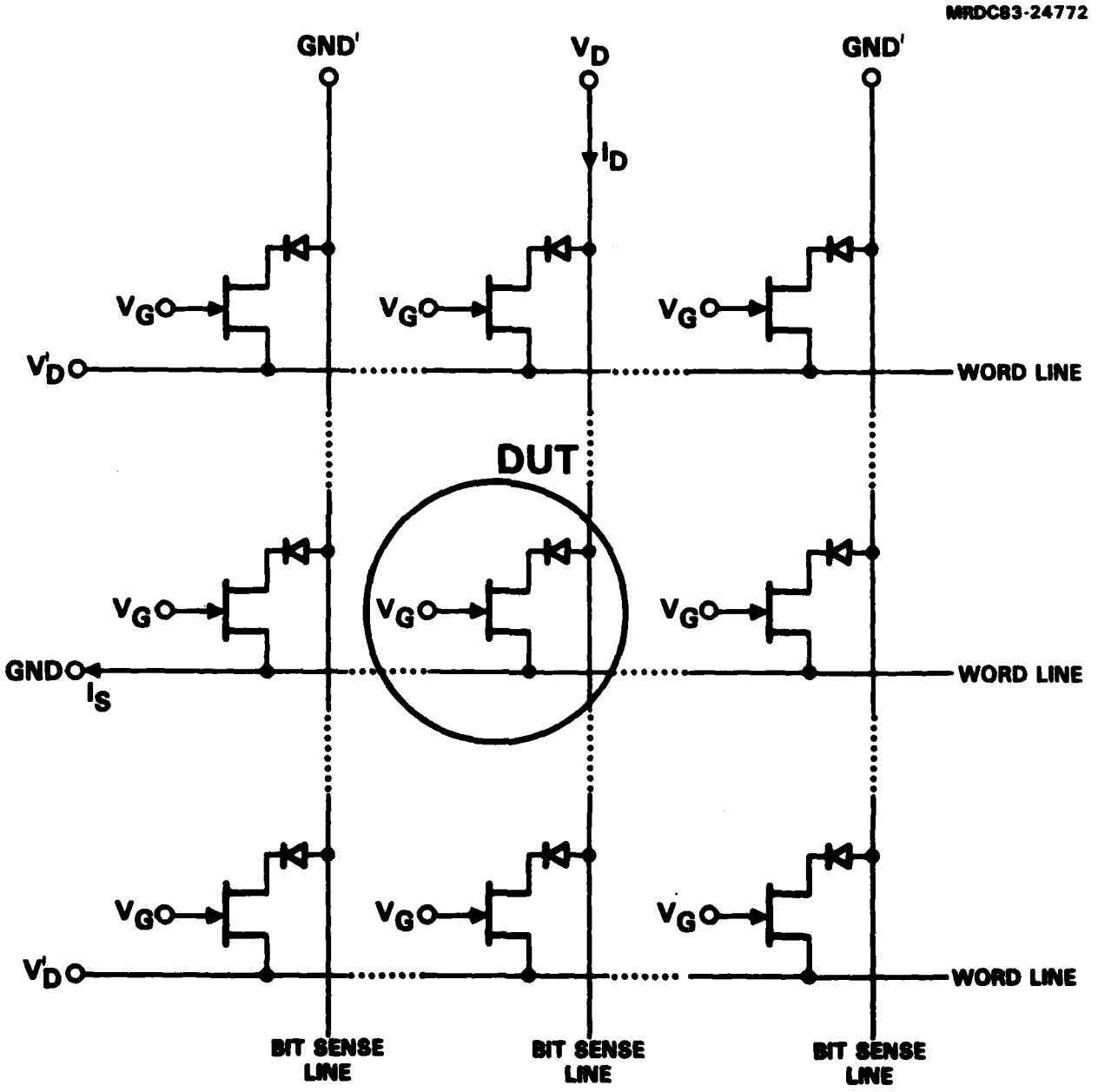

Fig. 6 Biasing scheme for testing a single output FET within an undecoded RAM array.

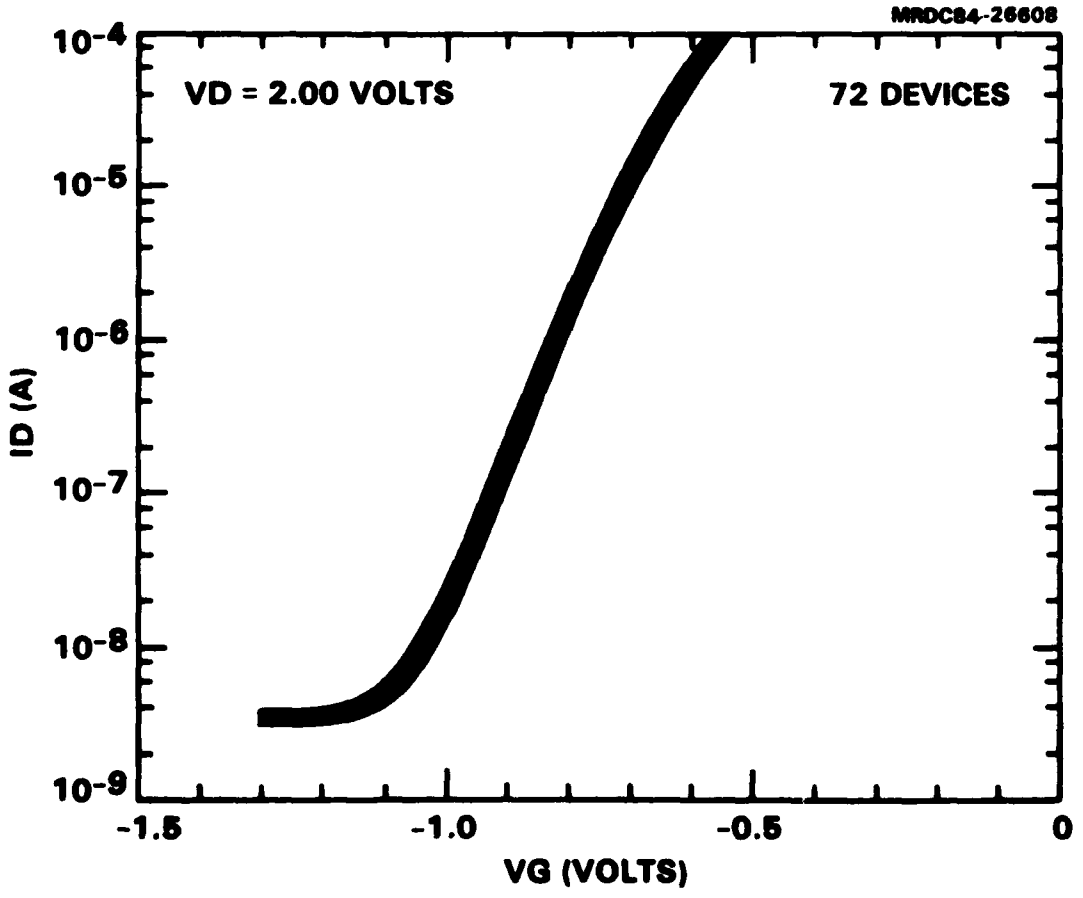

Fig. 7 Superimposed subthreshold characteristics of 72 FETs located in a 9 × 8 subarray of an uncoded RAM array. These data correspond to a high yield wafer.

this wafer averages -0.7 V. Note in the figure how the current drops exponentially (the voltage scale is logarithmic) with the gate voltage below threshold. This exponentially dropping current represents the subthreshold current. At sufficiently negative voltage, the exponential drop stops and the current becomes constant due to leakage. This leakage takes place between points in the cell and is much larger than the gate leakage typically observed in isolated test transistors.

Although the leakage current is representative of normal current leakage in the RAM cells, its magnitude, which in Fig. 7 is on the order of 4 nA, is misleading. Figure 6 shows clearly that the current I_d injected into the bit sense line will include the sum of the leakage current of all 16 FET devices on the column. The bias scheme used to turn off the other devices does not block the leakage currents of the other FETs in the column. Therefore, if we assume that the leakage current is the same for all the FETs, the actual leakage current is 1/16 of the 4 nA observed in Fig. 7, and falls well within the tolerance of the design.

The measurement technique described above was applied to all the undecoded arrays on two wafers having high and low yield of fully functional arrays, respectively. At the current levels between 0.1 and 10 nA, which represent the "off" current for this design, in general, the subthreshold characteristics of the devices on the good wafer appear parallel to one another with a voltage spread on the order of 50 mV, and sometimes as low as 35 mV, as is the case in Fig. 7. On the poor yield wafer, the subthreshold characteristics showed much larger voltage spreads, typically 100 to 150 mV. This difference suggests that having good threshold uniformity and obtaining good yield go hand in hand. However, attempts to observe direct correspondence between cell failures and anomalies in the characteristics of the transistors did not show such direct correlation. In some cases, a failed cell corresponded to a transistor that was open, or had an abnormal threshold voltage, or exhibited excessive leakage. However, even if the number of such clearly interpreted failures is multiplied by 3 to account for only one of the

three FETs in the cell being accessible to the measurement, only 10 to 20% of the observed cell failures can be accounted for. This is an indication that several factors are controlling the yield of RAM cells without a single one emerging, although subthreshold uniformity appears to be the most critical parameter.

4.0 TRANSMISSION GATE RAM

The transmission gate RAM circuit is one of three new RAM designs included on the RM-5 mask set. The goal of this particular design is to explore an alternate method of achieving two simultaneous objectives of radiation hardness and low power.

The overall dimensions of this circuit are 1600 μm × 1600 μm with the size if each memory cell is 43 μm × 63 μm. This RAM circuit has 256 cells, configured as 256 × 1, in 16 rows and 16 columns.

Each RAM cell consists of four depletion mode MESFETs, six diodes and four CERMET resistors. Two of the MESFETs are switching transistors used for data storage. The other two are the transmission gates, used for reading, and writing to/from the cell. Four of the diodes perform a level shifting function to provide the proper bias at the gates of the switching transistors. The other two diodes are reverse biased, and act as speed-up capacitors to facilitate rapid cell switching. They also provide a small contribution to preserving the data in the cell during a read operation. The CERMET resistors act as the passive load elements of the cell. They were chosen because their high sheet resistivity (3 MΩ/sq) makes them ideal for low power applications, and their relatively inert nature makes them ideal for radiation hardness.

The sense amplifiers and address buffers were designed using differential amplifiers. The one-sense amplifier per column configuration was chosen over the lower power option of having a single-sense amplifier for the entire array because the multiple sense amplifier approach allows for shorter interconnect lines between the sense amplifier and the memory cells. This results in lower capacitances on the lines which the low power memory cells must drive. Positive feedback is incorporated into each sense amplifier, which reinforces the data in the addressed cell. The price paid for the feedback is a slight reduction of the sense amplifiers' input sensitivity. Where the sense amplifiers accept differential inputs (data and its complement), and a single output is used, the address buffers have one of their

differential inputs connected to a DC reference voltage, and the two complementary outputs are used. This method allows for generating complementary signals with minimal timing skew between them.

All address signals and their complements are required by the row and column decoders. The row decoders were designed using SDFL, with the output connected to a source follower. This source follower controls the gates of the memory cell transmission transistors along a single row. The drains of all source followers on the row decoders are connected to an independent bonding pad to allow for adjustment of the bias applied to the transmission gates. SPICE simulations indicate that the circuits will be very sensitive to the voltage swings applied to the transmission gates. If the high level is high enough to forward bias the gate of the transmission transistor, the control signal can conduct to the memory cells and destroy the data. At the same time, the level must be high enough to ensure that the transmission gate is turned on, so that desired data can be written to or read from the cell.

The column decoders also use Schottky diodes to perform the combinatorial logic function. Unlike conventional SDFL, the resultant signal at the drain of the pulldown transistor is used to control the gates of multiple (three independent) switching transistors. One of the switching transistors is wired ORed with the output of the sense amplifier, to control the data seen at the output stage. The other two switching transistors control the gates of the source follower column drivers, in conjunction with the data and write enable control circuitry. The data and write enable control circuits were designed in a fashion similar to the column decoders. Sixteen independent switching transistors are controlled by the logic combination (OR) of the data and write enable; one transistor for each column. Another sixteen transistors are controlled by the logic combination using the complement of data in.

The advantage of controlling multiple inputs in this fashion is that a minimum number of components are required to perform complicated logic functions. The lowered component count increases reliability and offers reduced power consumption. We have seen that the susceptibility of conventional SDFL

circuits to upsets caused by transient ionizing radiation can be greatly reduced by adjusting the bias voltage (V_{pd}) on the gates of the pulldown transistors. The same should also hold true for this circuit implementation. The disadvantage of this implementation is that the driving node is not ideally suited to rapidly charge and discharge the high capacitive load of the switching transistors and their associated interconnects. This means that the high speed performance of this circuit will be compromised. Since low power operation and radiation hardness are the most important specifications of this design, the tradeoff is warranted.

Some design features were not included in this circuit. Address transition detection circuitry, which would provide a more reliable means of nondestructively reading the data, was not included because the high power overhead associated with the implementation of this rather complicated design feature would defeat the main goals being pursued. Power switching circuitry was also omitted from this design in order to minimize additional complications, and because several variations of power switching circuitry are being included on other RAM designs.

This RAM circuit was designed to operate with a nominal threshold voltage of -0.5 V and a CERMET sheet resistivity of 3 MΩ/sq. With these parameters, the estimated power requirements are 3.5 μW/cell, and 96 mW/ powered up circuit. Since this circuit resides on a mask containing other RAM designs requiring different parameters, we will be able to explore the effect of several process variations on this design, when wafers are processed to meet their requirements. The variation with the most promise is the one with the CERMET sheet resistivity lowered to 100 KΩ/sq. SPICE simulations indicate that memory cells with the lower resistor values will operate faster, and will be less sensitive to disturbances introduced through the transmission gates during read operations. Unfortunately, the lowered resistor values also result in much higher power dissipation. We will also be able to evaluate circuits with higher threshold voltages. These circuits will have reduced

noise margins and will require higher power, but they promise improved speed performance. Wafers with several combinations of threshold voltage and CERMET resistivity will be available for evaluation.

Several diagnostic circuits were also included on the mask set to facilitate identifying problem areas. These include a 256 bit undecoded RAM circuit; the 16 input NOR gate at the RAM output state; a single memory cell with internal points brought to bonding pads; all peripheral circuitry with no memory cells; sense amplifiers; and differential amplifier address buffers.

Several wafers have already been fabricated and now await testing. The probe cards have been received and the edge connector has been wired. Since this design is configured differently from previous RAM designs, minor modifications will have to be made to test apparatus before testing can begin.